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1. A system for testing a first integrated circuit chip to be packaged along with at least a second integrated circuit chip in a semiconductor device, wherein at least some external terminals for the semiconductor device are to be shared by the first and second integrated circuit chips, wherein the first integrated circuit chip is designed for normal operation and a test mode, the system comprising on the first integrated circuit chip:

a first bonding pad for a SET signal;

a second bonding pad for a LOAD signal;

a third bonding pad for a TEST signal; and

a plurality of bonding pads for TDQ signals;

wherein the SET, LOAD, and TEST signals are used to transition the first integrated circuit chip from normal operation into the test mode and to enable test codes to be loaded into the first integrated circuit during a programming phase of the test mode;

wherein the TDQ signals are used to load test codes into the first integrated circuit during the programming phase and to read/write data to and from the first integrated circuit during an access phase of the test mode.

2. The system of Claim 1 wherein in the access phase the first integrated circuit chip is operated to test for functionality.

3. The system of Claim 1 wherein in the access phase the first integrated circuit chip is further operated to test for ability to withstand stresses.

4. The system of Claim 1 wherein the first integrated circuit chip comprises a memory device.

5. The system of Claim 1 wherein the first integrated circuit chip comprises a logic device.

6. The system of Claim 1 wherein the first integrated circuit chip comprises a plurality of test input control buffer circuits, each test input control buffer circuit operable to receive at least one of the TDQ signals for loading test codes into the first integrated circuit chip during the programming phase; and wherein the SET, LOAD, and TEST signals control the test input control buffer circuits.

7. The system of Claim 1 wherein the SET signal is used to set a test code and a LOAD signal is used to load the test code during the programming phase.

8. The system of Claim 1 wherein the first, second, and third bonding pads for the SET, LOAD, and TEST signals and the plurality of bonding pads for corresponding TDQ signals are implemented on the first integrated circuit chip; and wherein at least a portion of the SET, LOAD, TEST, and TDQ signals can be multiplexed with signals at other bonding pads of the first integrated circuit chip.

9. The system of Claim 1 wherein the first, second, and third bonding pads for the SET, LOAD, and TEST signals and the plurality of bonding pads for corresponding TDQ signals are operable to be connected to external testing circuitry.

10. A memory chip for packaging along with at least a system chip in a semiconductor device, wherein at least some external terminals for the semiconductor device are to be shared by the memory chip and the system chip, wherein the memory chip is designed for normal operation and a test mode, the memory chip comprising:

a first group of bonding pads for communicating TEST, SET, and LOAD signals operable to transition the first integrated circuit chip from normal operation into the test mode and to enable test codes to be loaded into the memory chip during a programming phase of the test mode; and

a second group of bonding pads for communicating a plurality of TDQ signals operable to load test codes into the memory chip during the programming phase and to read/write data to and from the memory chip during an access phase of the test mode.

11. The memory chip of Claim 10 comprising a third group of bonding pads for communicating a plurality of test control signals operable to control the memory chip during the access phase of the test mode.

12. The memory chip of Claim 11 wherein each test control signal corresponds to a respective control signal that is used to control the memory chip during the normal operation.

13. The memory chip of Claim 11 wherein each of the test control signals is multiplexed with the respective control signal.

14. The memory chip of Claim 11 wherein the test control signals comprise test write enable (TWE), test row address strobe (TRAS), and test column address strobe (TCAS) signals.

15. The memory chip of Claim 10 wherein in the access phase the memory chip is operated to test for functionality.

16. The memory chip of Claim 10 wherein in the access phase the memory chip is operated to test for ability to withstand stresses.

17. The memory chip of Claim 10 comprising a plurality of test input control buffer circuits, each test input control buffer circuit operable to receive at least one of the TDQ signals for loading test codes into the memory chip during the programming phase, and wherein the SET, LOAD, and TEST signals control the test input control buffer circuits.

18. A first integrated circuit chip for packaging along with at least a second integrated circuit chip in a semiconductor device, wherein at least some external terminals for the semiconductor device are to be shared by the first and the second integrated circuit chips, wherein the first integrated circuit chip is designed for normal operation and a test mode, the first integrated circuit chip comprising up to eleven bonding pads for complete testing of the first integrated circuit chip, wherein the up to eleven bonding pads are for communicating TEST, SET, LOAD, and a plurality of TDQ signals, wherein the TEST, SET, and LOAD signals are operable to transition the first integrated circuit chip from normal operation into the test mode and to enable test codes to be loaded into the first integrated circuit chip during a programming phase of the test mode, and wherein the plurality of TDQ signals are operable to load test codes into the first integrated circuit during the programming phase of the test mode and to read/write data to and from the first integrated circuit chip during an access phase of the test mode.

19. The first integrated circuit chip of Claim 18 wherein at least a portion of the SET, LOAD, TEST, and the plurality of TDQ signals can be multiplexed with signals at other bonding pads of the first integrated circuit chip.

20. The first integrated circuit chip of Claim 18 wherein the bonding pads for complete testing of the first integrated circuit chip are operable to be connected to external testing circuitry.

21. The first integrated circuit chip of Claim 18 wherein in the access phase the first integrated circuit chip is operated to test for functionality.

22. The first integrated circuit chip of Claim 18 wherein the loading of test codes into the first integrated circuit chip is performed asynchronously.

23. A system for testing a first integrated circuit chip to be packaged along with at least a second integrated circuit chip in a semiconductor device, wherein at least some external terminals for the semiconductor device are to be shared by the first and second integrated circuit chips, wherein the first integrated circuit chip is designed for normal operation and a test mode, the system comprising up to eight bonding pads on the first integrated circuit chip for receiving corresponding TDQ signals, wherein the TDQ signals are used to load test codes into the first integrated circuit during a programming phase of the test mode and to read/write data to and from the first integrated circuit during an access phase of the test mode.

24. The system of Claim 23 wherein in the access phase the first integrated circuit chip is operated to test for functionality.

25. The system of Claim 23 wherein in the access phase the first integrated circuit chip is further operated to test for ability to withstand stresses.

26. The system of Claim 23 wherein the first integrated circuit chip comprises a memory device.

27. The system of Claim 23 wherein the first integrated circuit chip comprises a logic device.

28. The system of Claim 23 wherein the first integrated circuit chip comprises a plurality of test input control buffer circuits, each test input control buffer circuit operable to receive at least one of the TDQ signals for loading test codes into the first integrated circuit chip during the programming phase.

Claims 29 through 32 are cancelled